Telescopio Nazionale Galileo

Batman: Acquisition system (test and settings)

Document version 1.0

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Change Record

Issue/ Rev.	Date	Section/Page affected	Reason/Remarks
V1.0	June 2016	First version	draft
V1.1	22/12/2026		

Contents

Introduction

1.1 Scope

This document is a report of electronics part of the acquisition system, including the tests on the detectors. The performance if the software system will be described in another document.

1.2 Additional information

No additional information, at the moment.

1.3 Contact information

Feedback on this document is encouraged. Please email to cosentino@tng.iac.es

1.4 Reference documents

[RD01] **E2V datasheet: CCD42-80 Back Iluminated Hight Performance CCD sensor**

[RD02] **TN 906/419 - The e2v Buttable CCD Package: Design & Mounting Philosophy**

[RD03] **Reference Data MIL-STD-681 Wire Color Code**

[RD04] **Datasheet: Straight Micro-D Solder Connector**

1.5 Applicable documents

Verification of the rack voltages

- Power on the rack without the CDS and SPC boards and test the power led
- Test the voltages by using the extension board and the **Error! Reference source not found.**and **Error! Reference source not found.**

Table 1 - P1 connector pinout and values

P1	Modified	Power board	color	connector	Sarg	Bat#1	Bat#2
A9	AGnd	J4:1,4,5,9,10	white	D			
A11	AGnd	J3:1,4,7,8	white	D			
A15	AGnd	J4:1,4,5,9,10	white	D			
A17	AGnd	J3:1,4,7,8	white	D			
A19	AGnd		white	D			
A31	-20 V	J3: 5	Green-red	S	-27 V	-27.86	-27.39
A32	+5 V	J2: 5,8,7	Red-blue	L			
B20	AGnd	J4:1,4,5,9,10	white	D			
B23	AGnd	J3:1,4,7,8	white	D			
B24	+15 V	J1: 4	Red-brown	K		17.73	17.72
B28	AGnd	J4:1,4,5,9,10	white	D			
B29	AGnd	J3:1,4,7,8	white	D			
B30	+32 V	J4: 8	Red	F			
B31	AGnd		white	D		32.77	32.62
B32	+5 V	J2: 5,8,7	Red-blue	L		5	4.98
C9	AGnd		white	D			
C10	+15				+15 V	17.71	17.71
C11	+15				+15 V	17.71	17.71
C31	+20 V	J3: 6	Blue	N	+27 V	27.3	27.09
C32	+5 V	J2:5,8,7	Red-blue	L		5.42	4.99

Table 2 - P2 connector pinout and values

P2	Modified	Power board	color	connector	Sarg	Bat#1	Bat#2
A9	AGnd		white	D			
A11	AGnd	J4:1,4,5,9,10	white	D			
A15	AGnd	J3:1,4,7,8	white	D			
A17	AGnd		white	D			
A19	AGnd		white	D			
A24	JP3						
A25	JP4						
A26	NC						
A27	JP5						
A31	-8 V	J4: 2	Red-black	E	-13 V	-13.52	-13.22
A32	+5 V	J2: 5,8,7	Red-blue	L		5.42	4.99
B1	+12				+ 5 V	5.42	4.99
B2	JP6						
B13					+ 5 V	5.42	4.99
B21					+ 4.76	5.42	4.99
B20	AGnd	J4:1,4,5,9,10	white	D			
B23	AGnd	J3:1,4,7,8	white	D			
B24	+24	J1:9	orange	B		27	26.25
B25	-12	J1:5	Yellow-red	H		-12	-12
B26	+12	J1:4	Red-brown	K	+5 V	5	5
B27	TGND	J1:6,8,10	White-red	U			
B28	DGND	J2: 9,6,10	Black	A			
B29	DGND	J2: 9,6,10	Black	A			
B30	+32 V	J4: 8	Red	F		32.77	32.61
B31	DGND	J2: 9,6,10	Black	A			
B32	+5 V	J2: 5,8,7	Red-blue	L		5.42	4.99
C9	AGND		white	D			
C10	+24				26 V	26.57	26.25
C11	+24				26 V	26.57	26.25
C17	TGND	J1:6,8,10	White-red	U			
C24	NC						
C27	JP10						
C31	+8 V	J4:3	Yellow	P	13 V	13.26	13.12

C32	+5 V	J2: 5,8,7	Red-blue	L		5.42	4.99

Verification of the Bias and Clock voltages

- Insert the SPC, CDS, cables, bias board and clock board and test the boot, the bias and clock voltages by using the telemetry and tester
  a. Use the following configuration files:
    i. MaxVoltagesBiasClock.ccd
    ii. MeanVoltagesBiasClock.ccd
    iii. MinVoltagesBiasClock.ccd
  b. For each configuration read the telemetry and capture the results
  c. For each configuration read the values with the tester and write the result in the corresponding table.

1.6 Biases voltages on the preamplifier board (20/06/2016)

The preamplifier board ...

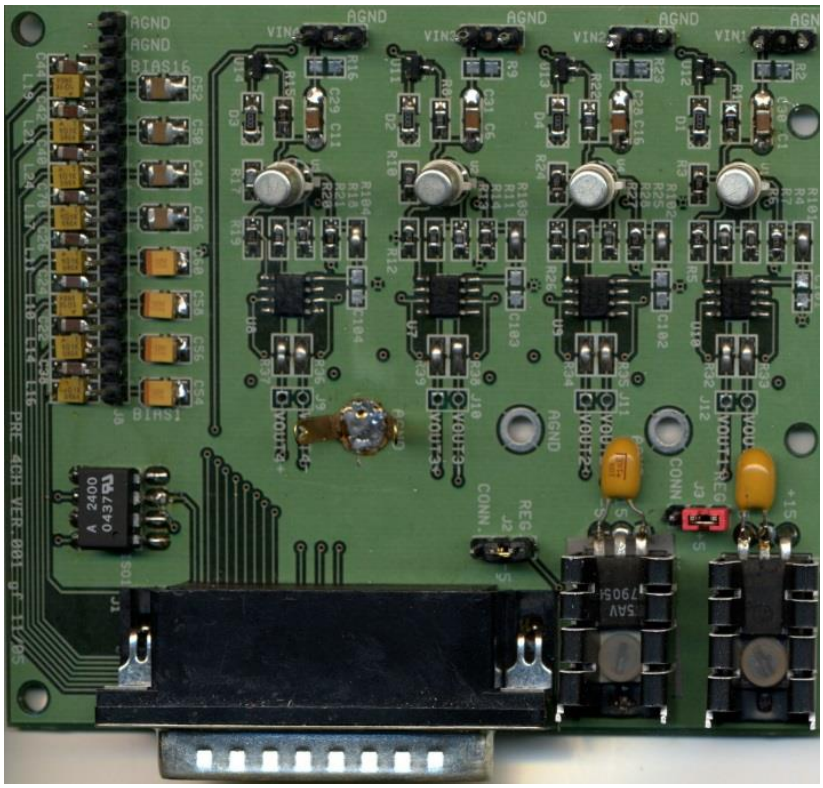


Figure 1 - The preamplifier

Rack# 1	Pre# 5	CDS# 6	SPC# 9

Table 3 - Bias Values

Bias#	Min	Med	Max	OK	Note
1	15.02	22.06	30.12		
2	15.02	22.06	30.11		
3	15.06	22.10	30.14		
4	14.28	21.75	30.20		
5	4.99	8.99	14.99		
6	4.99	8.99	14.99		

7	4.99	8.99	14.98		
8	4.99	8.99	14.98		
9	-4.99	0	4.99		
10	-4.99	0	4.99		
11	-4.99	0	4.99		
12	-4.99	0	4.99		
13	-9.99	0	9.99		
14	-9.99	0	9.99		
15	-9.99	0	9.99		
16	-9.99	0	9.99		

1.7 Clock voltages (20/06/2016)

1) Test the clock values in the High and low state
    a. Use the following configuration files:
        i. testctrl_hi.ccd
        ii. testctrl_low.ccd
    b. For each configuration read the telemetry and capture the results
    c. For each configuration read the values with the tester and write the result in the corresponding table.

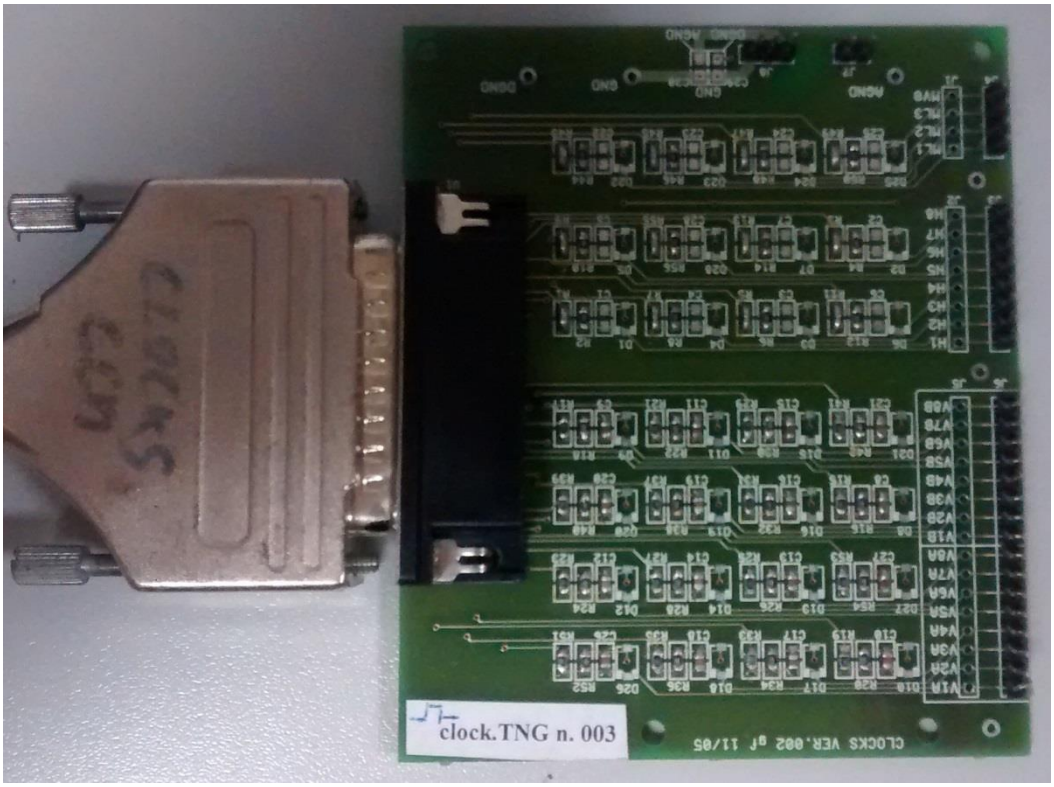


Figure 2 - Clock board

Rack# 1	**Clock#3**	**CDS#6**	**SPC#9**

Table 4 - Clock values

Clock#	Min	Med	Max	OK	Note
h1	-9.41		9.69		
h2	-9.41		9.67		
h3	-9.39		9.70		
h4	-9.39		9.64		

h5	-9.38		9.57		
h6	-9.40		9.70		
h7	-9.38		9.59		
h8	-9.38		9.07		
V1	-9.39		9.60		
V2	-9.38		9.56		
V3	-9.43		9.66		
V4	-9.40		9.63		
V5	-9.43		9.70		
V6	-9.38		9.61		
V7	-9.40		9.60		
V8	-9.38		9.71		

1.8 Bias and clock telemetry

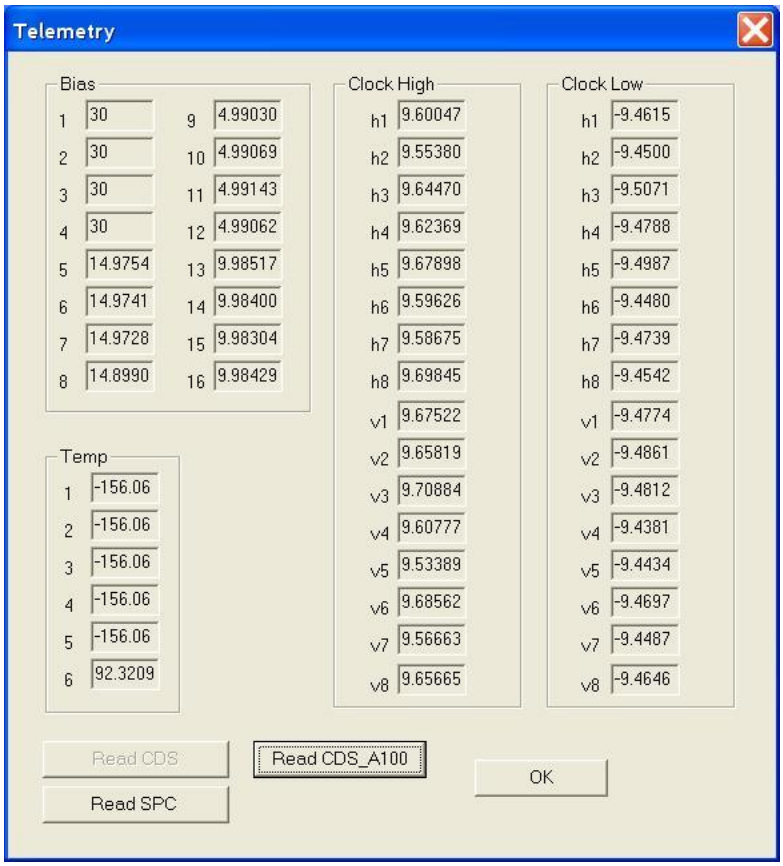


Figure 3 Telemetry of the maximum voltage values value provided by the CDS#6 and SPC#9 boards

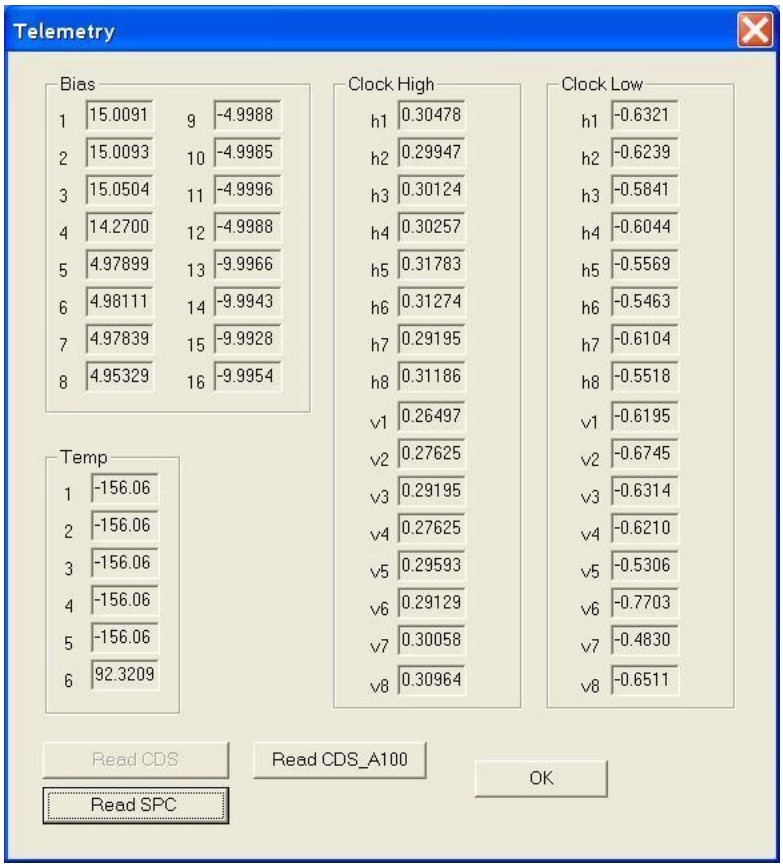


Figure 4 - Telemetry of the minimum voltages values provided by the CDS#6 and SPC#9 boards

Clock waveform test

- Test the waveform at the clock board output
    a. Use the “testfasi.ccd” configuration file
    b. Test the horizontal phases with the oscilloscope (time = 500 nSec or 1µsec)
    c. Test the vertical phases with the oscilloscope (time= 20 µsec or 50 µsec)
    d. save the results and put in this report

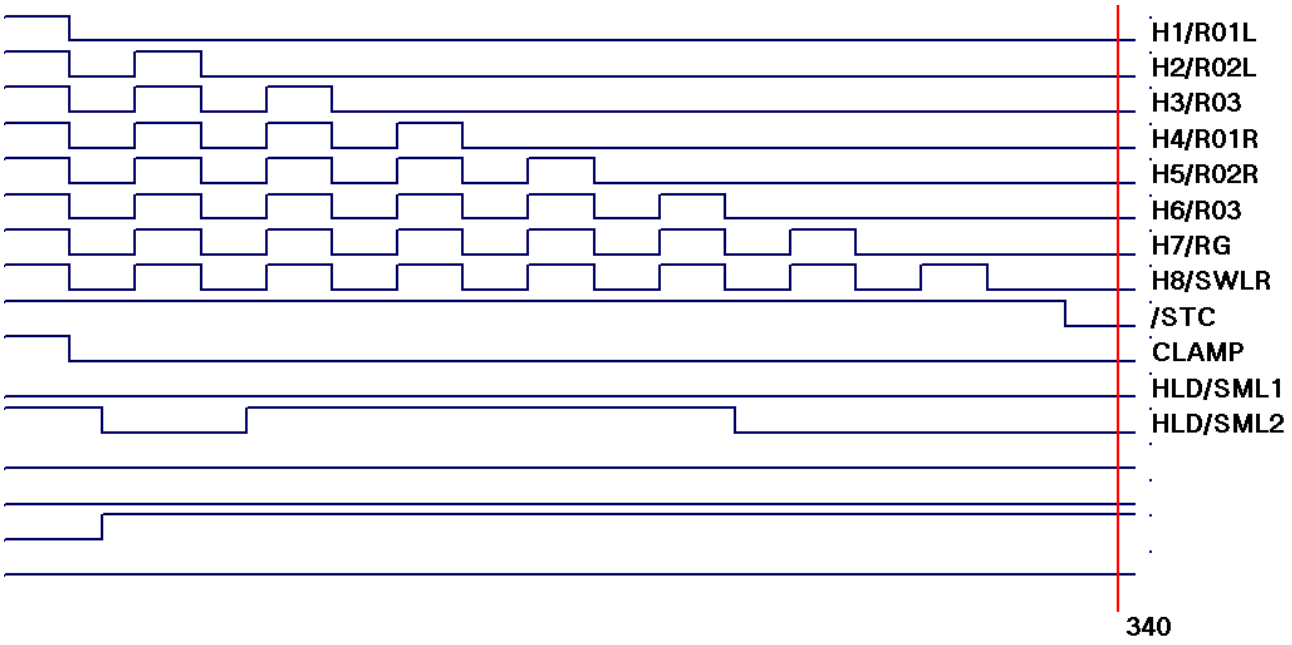


Figure 5 - Phases for the Horizontal clock test

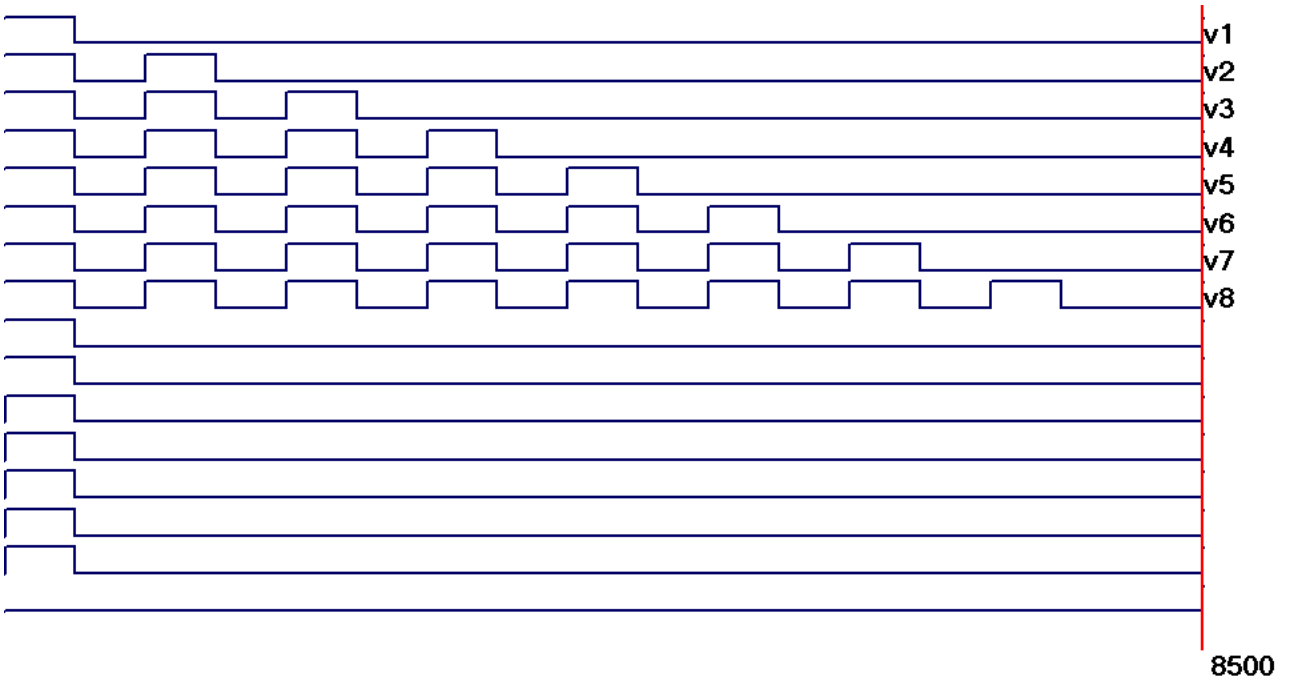


Figure 6 - Phases for the vertical clock test

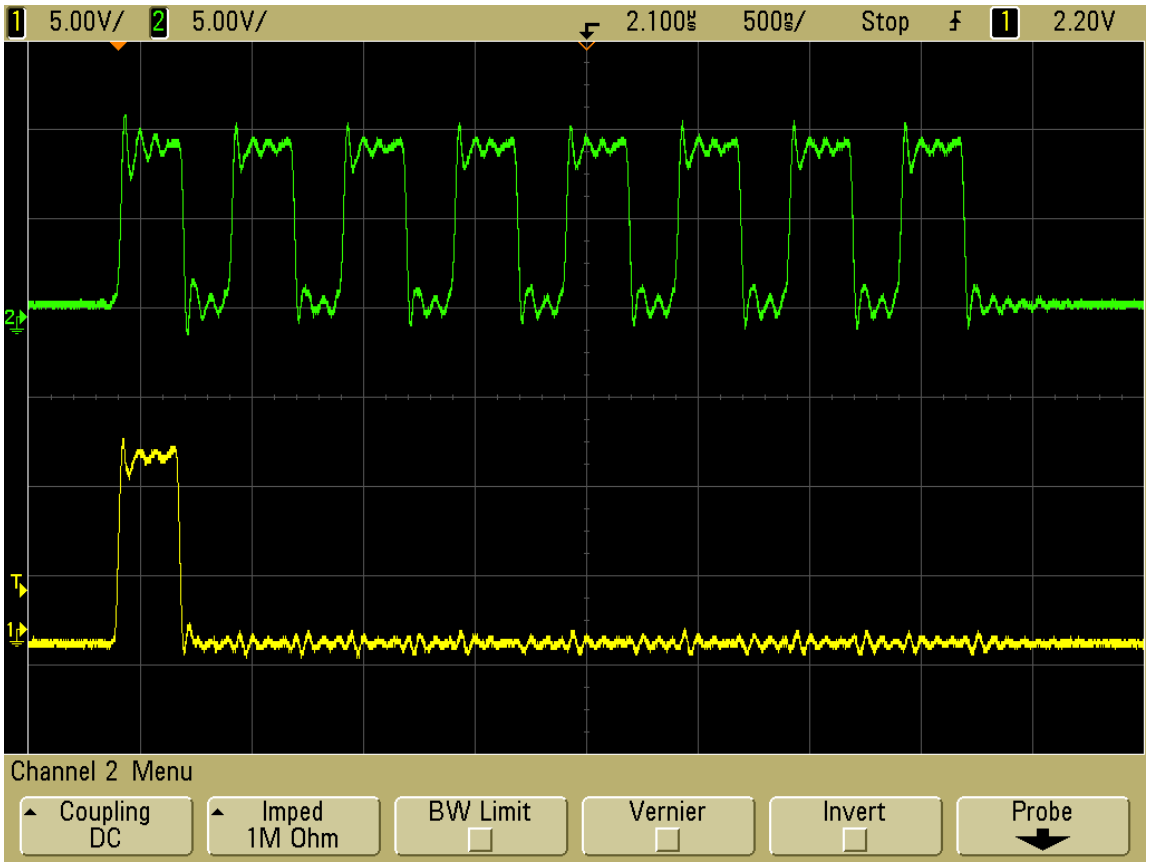


Figure 7 - Horizontal clock sample of H1 and H8

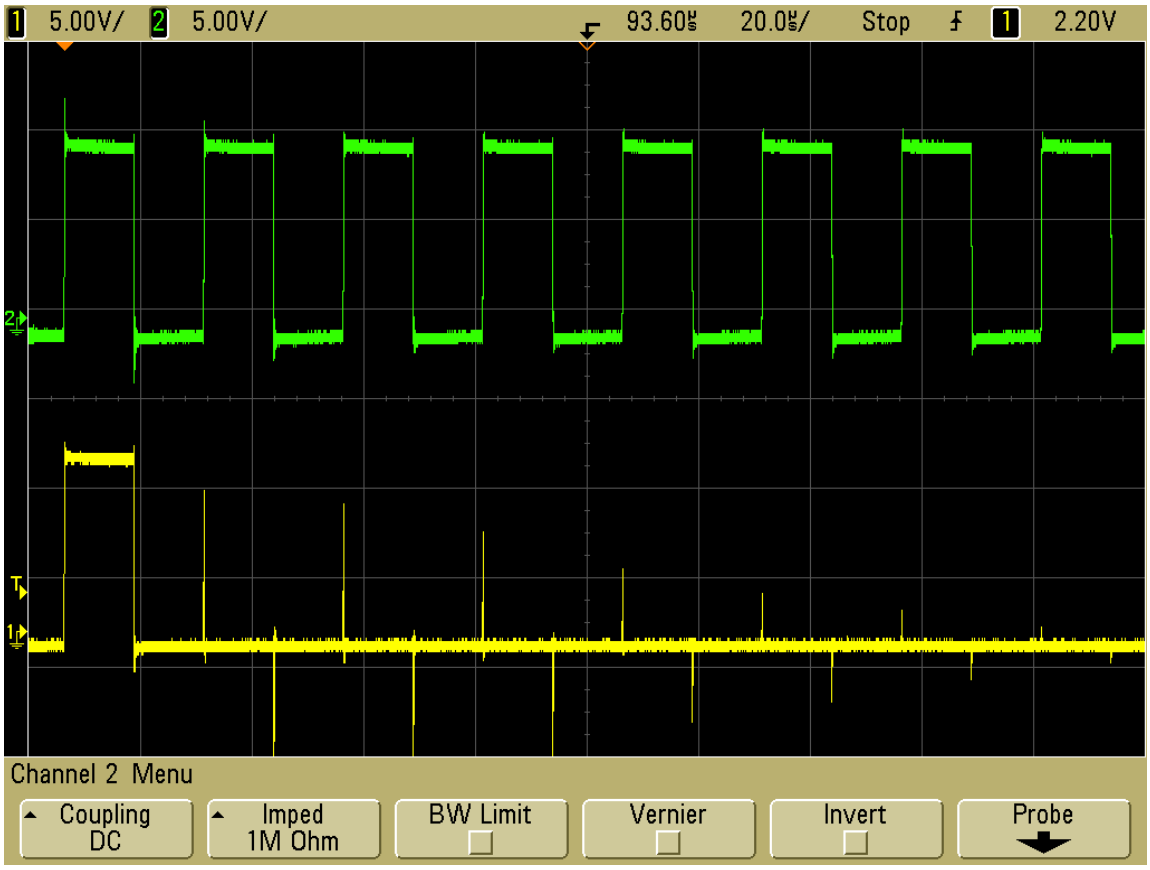


Figure 8 - vertical clock sample of V1 and V8

CCD phases test

a. use a real ccd configuration file
b. test the horizontal phase overlap and shape
c. test the vertical phase overlap and shape

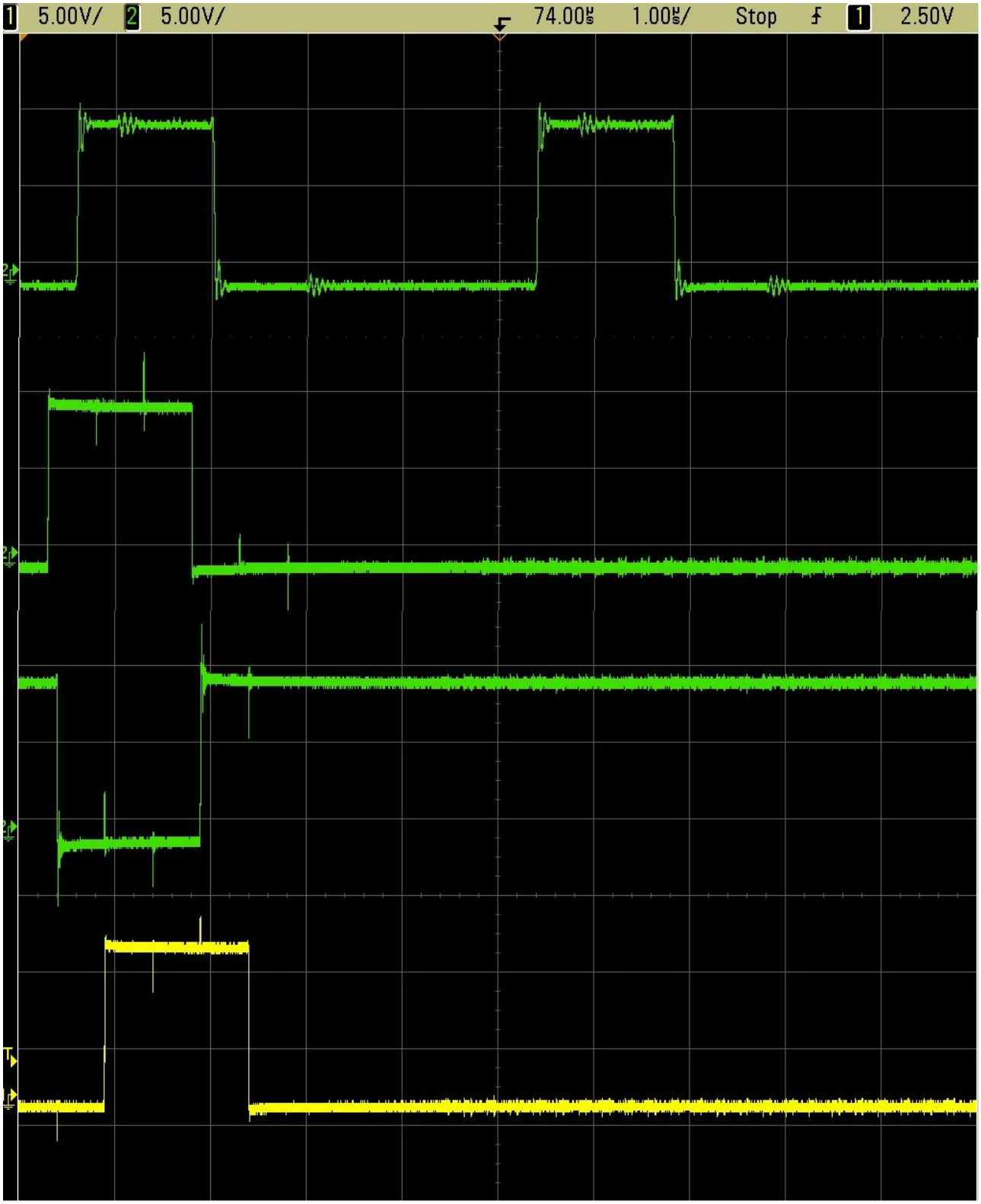


Figure 9 - Vertical phases of the CCD 4280 in both reading mode

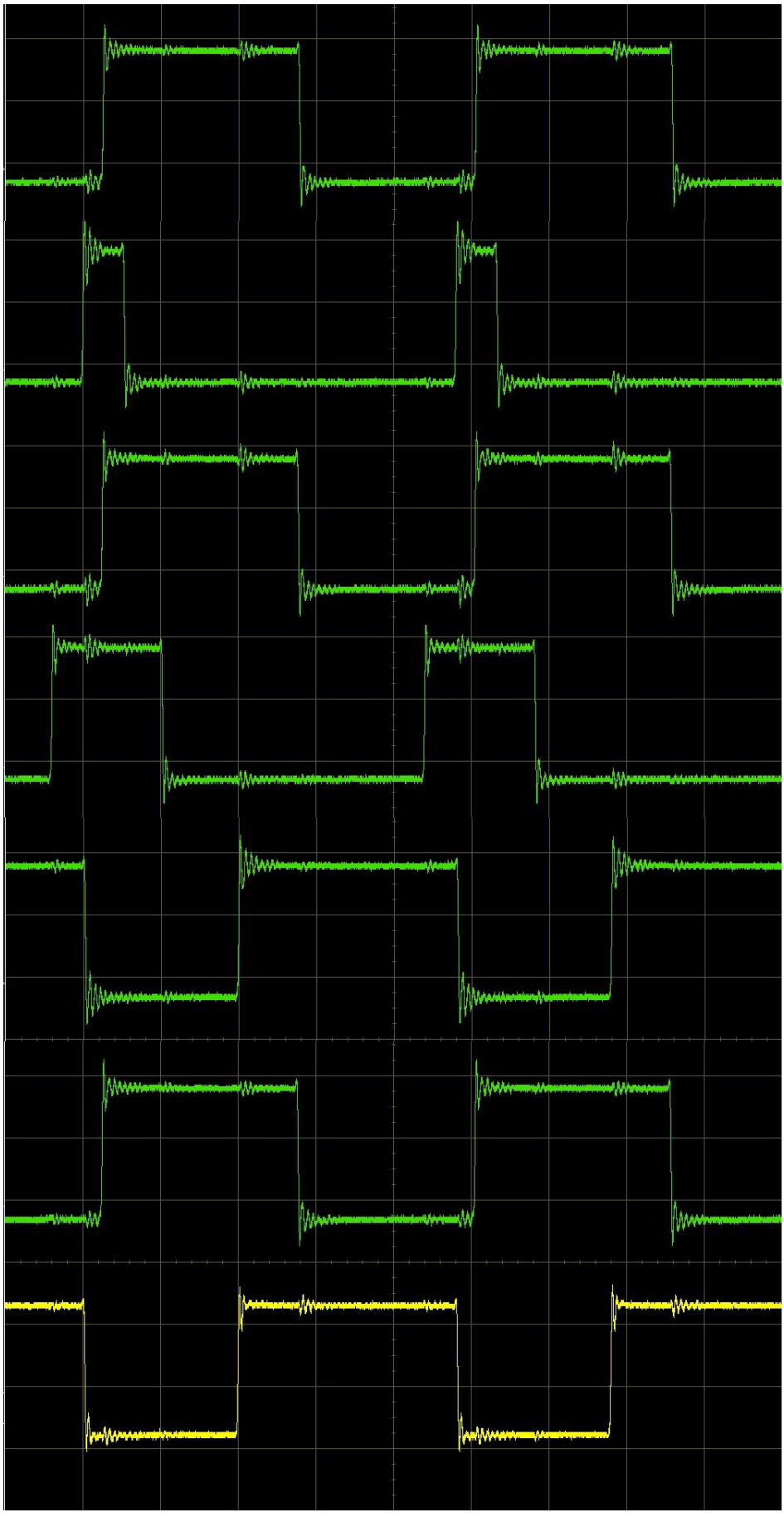


Figure 10 - Horizontal phases of the CCD 4280 in both reading mode

Preamplifier and CDS gains

Equipment:
Oscilloscope
Waveform generator (100Mvpp, 300KHz, square waveform)
Cable to connect the wave generator to the preamplifier

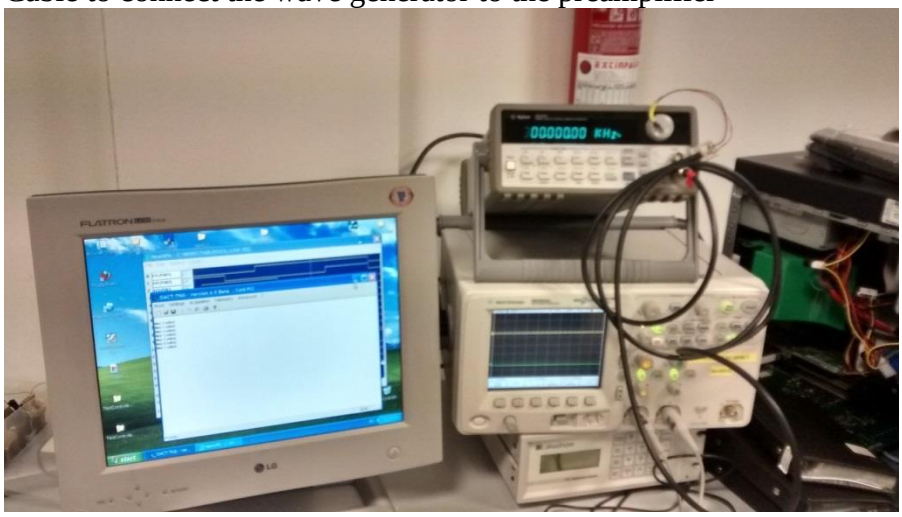


Figure 11 - equipment to measure the gain on the chain

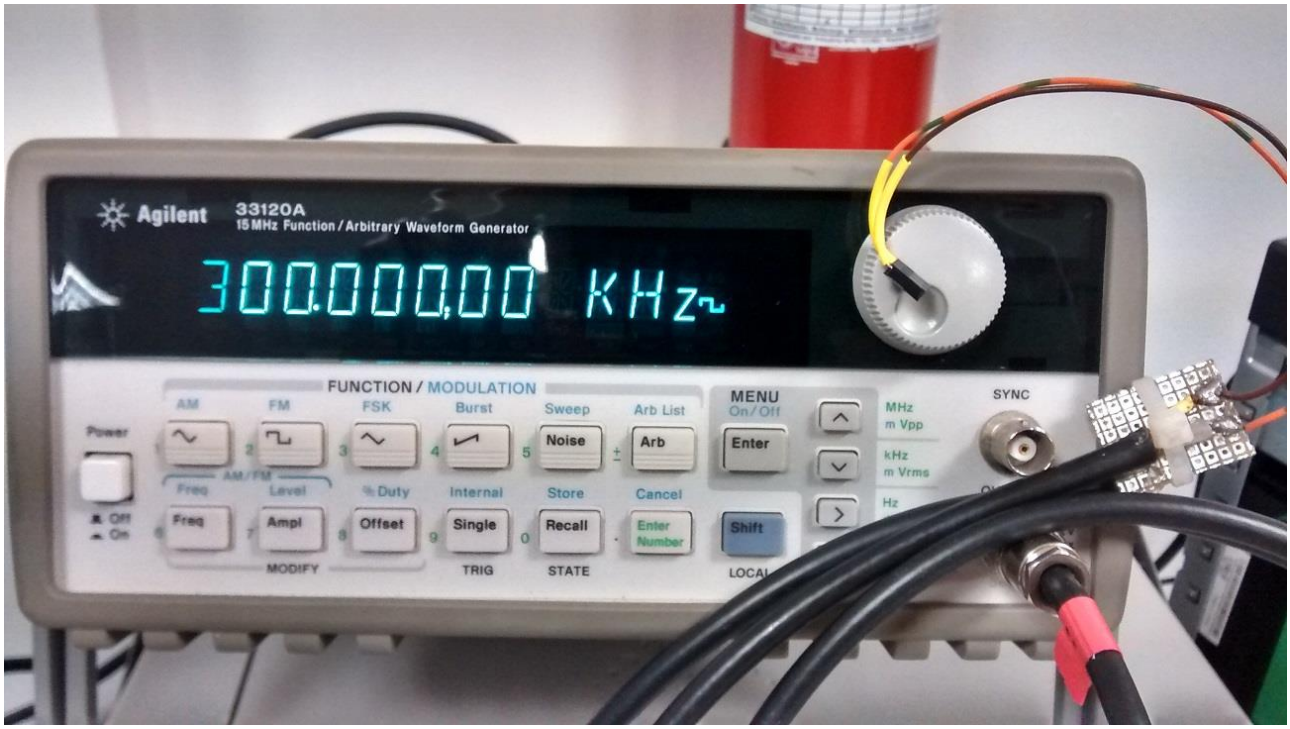


Figure 12 - Waveform generator and cable

Channel #	OK	Pre Gain	CDS-G1 Gain	CDS-G2 Gain	CDS-G3 Gain	ADC
1		3.9	3.3	6	10.5	0.5
2						
3						
4						

1. Calculated gain and conversion factor

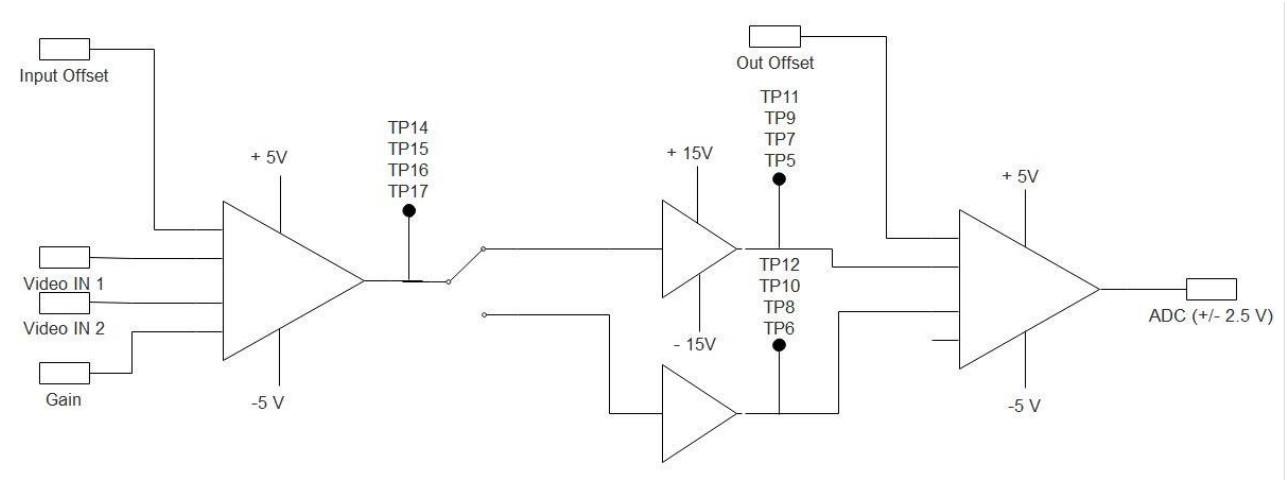


Figure 13 - Signal processing chain

The gain of the *whole* system is : G = 0.5 * Pre Gain * CDS-Gx Gain

CDS-G1 Gain = → Total gain = 6.5
CDS-G2 Gain → Total gain = 11.7
CDS-G3 Gain = → Total gain = 20.5

If the CCD sensitivity is 4.5 µV/e the corresponding voltages at the ADC input is:

G1 ----> 29.3 µV/e
G2 ----> 52.7 µV/e
G3 ----> 92.3 µV/e

The conversion factor of the ADC depends on the conversion range (bipolar input range +/- 2.5 Volts) and the resolution (16 bit = 65535 values).

$CF_{ADC} = 5 / 2^{16} = 76$ µV/ADU

The calculated conversion factor of the CCD is:

G1 ----> 2.6 e/ADU
G2 ----> 1.44 e/ADU
G3 ----> 0.82 e/ADU

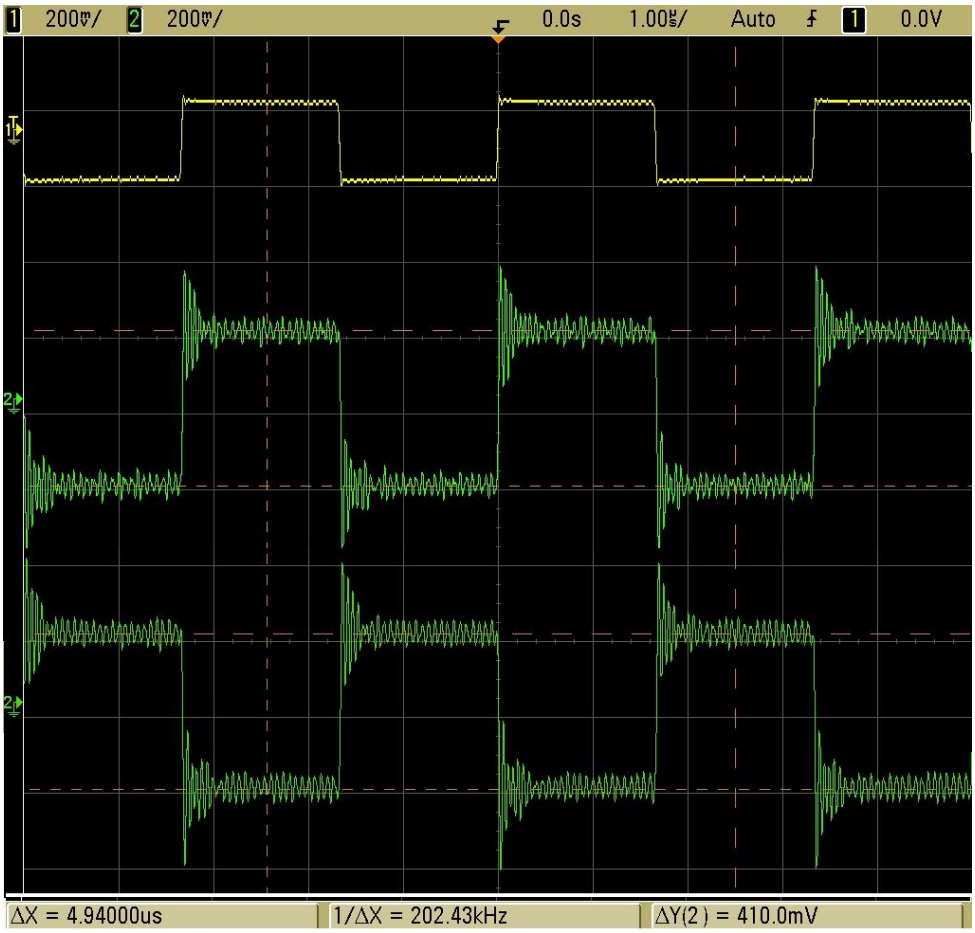


Figure 14 - waveform generator (yellow) and preamplifier outputs (green)

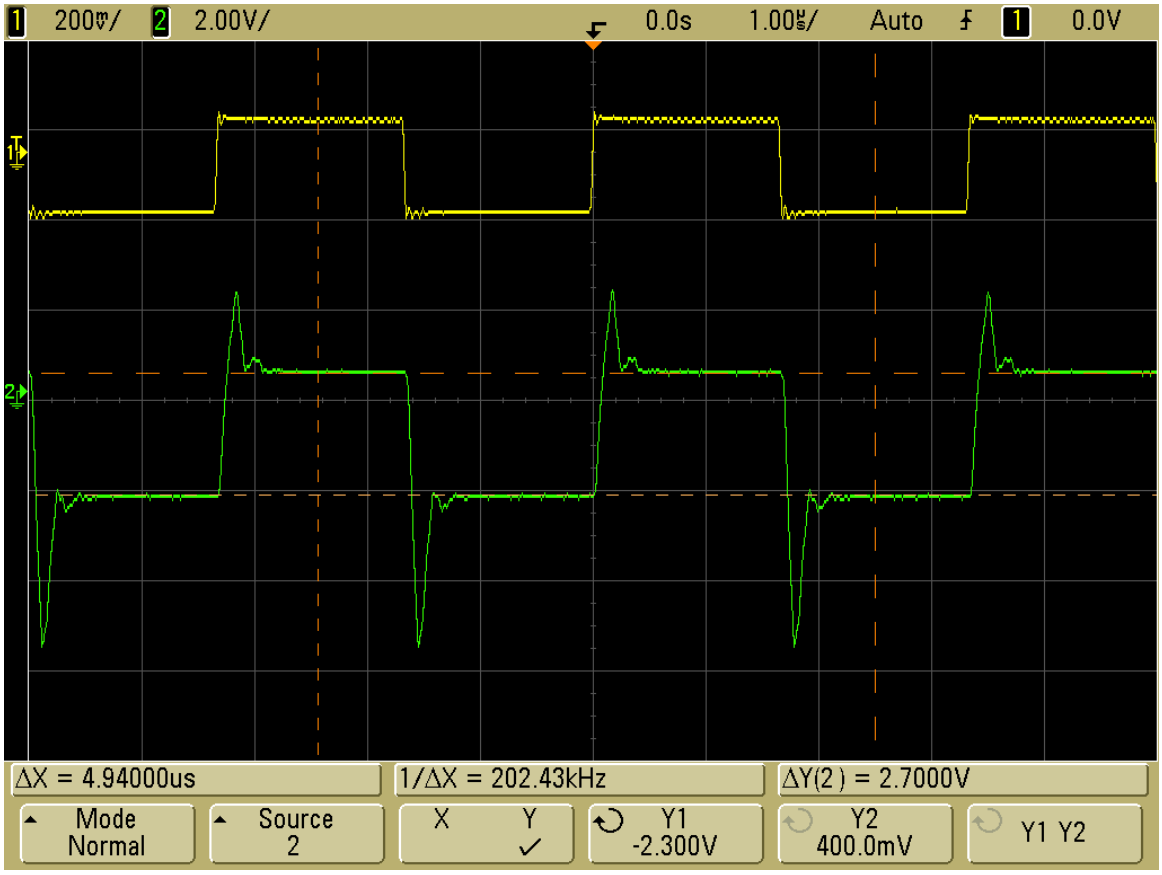


Figure 15 – CDS output - Gain 1-filter 0 (test point 1)

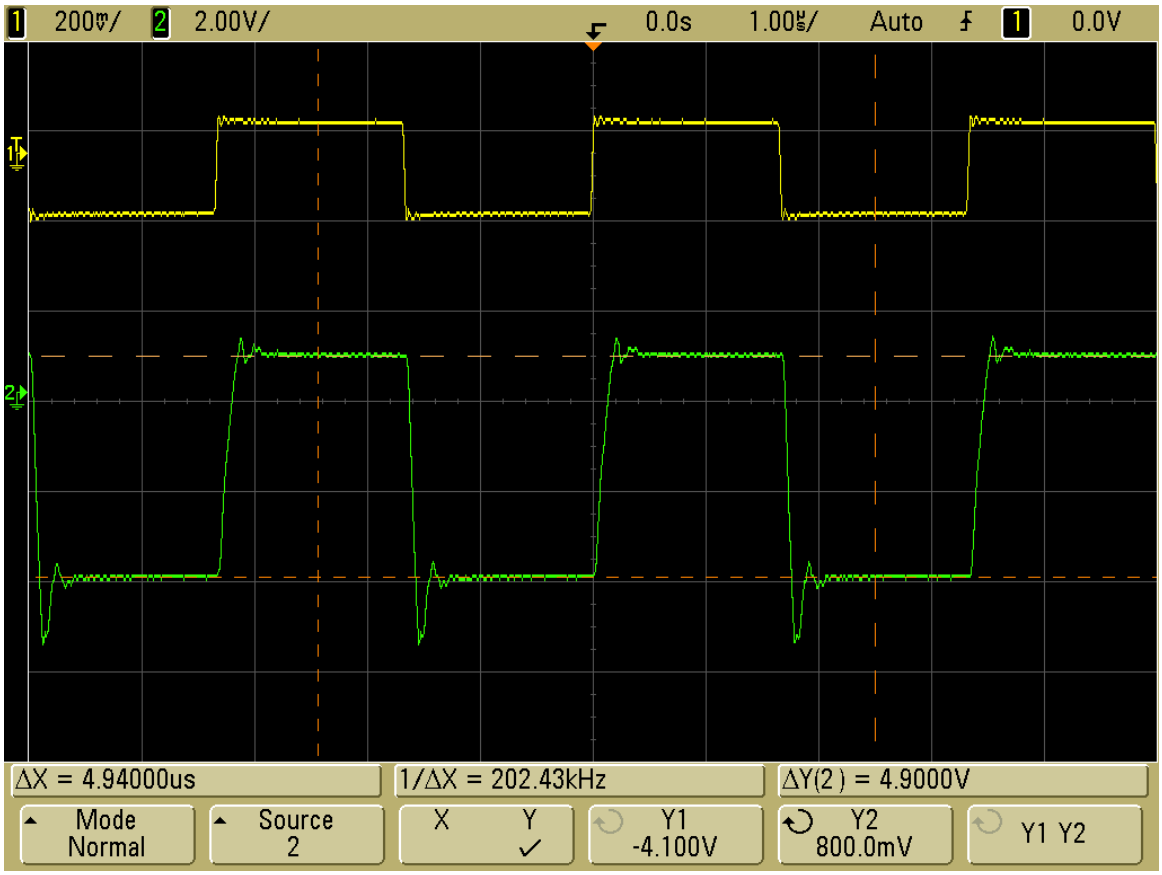


Figure 16 - CDS output Gain 2 – filter 0 (test point 1)

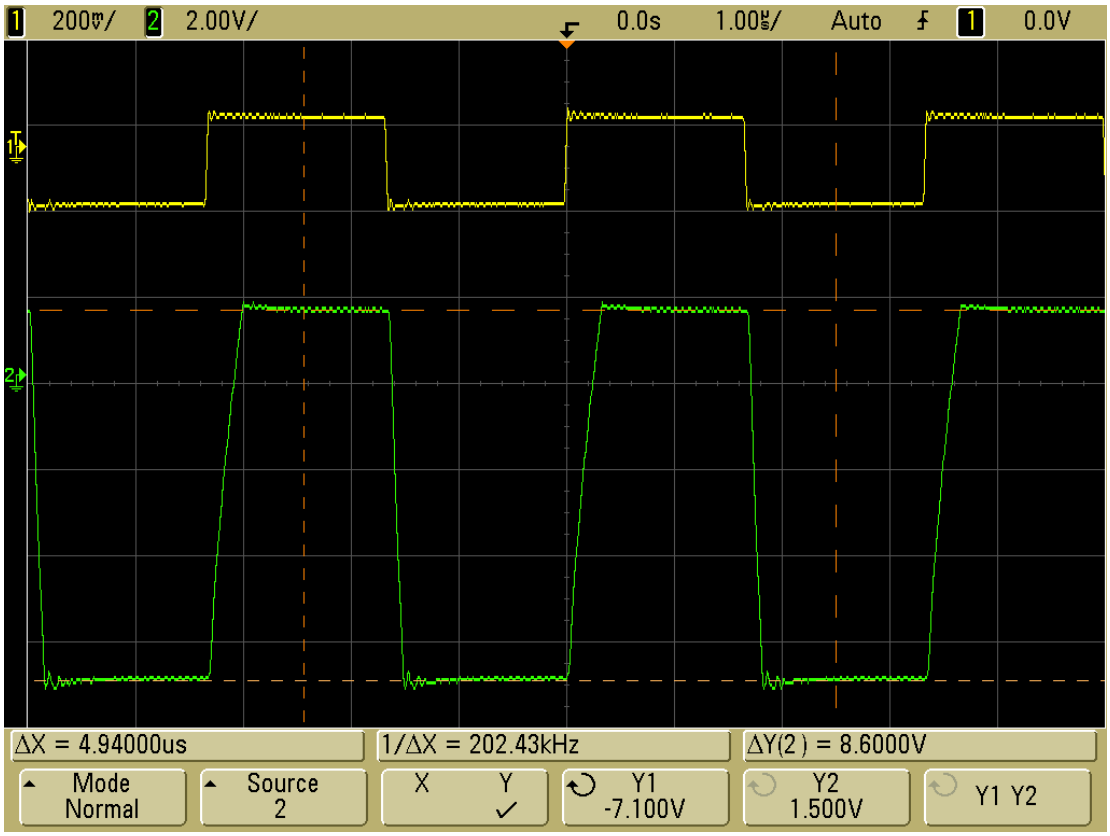


Figure 17 - CDS output Gain 3 filter 0 (test point 2)

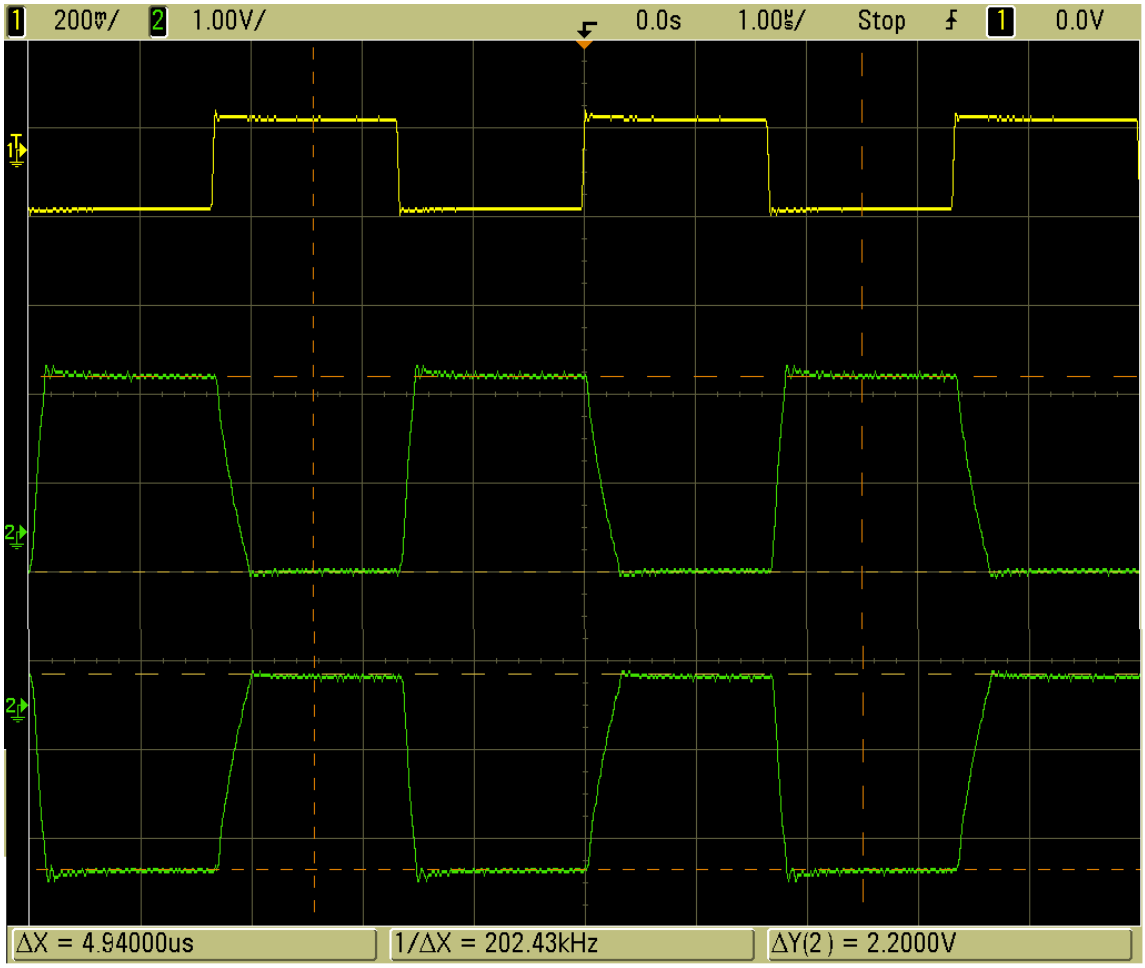


Figure 18 - Signals at the ADC input

Test with the CCD simulator cable

The CCD simulation configuration uses the ccdsimul.wfN horizontal phases and the CCDsimul.ccd configurations file together with the “simulator cable” and the preamplifier and clock boards.

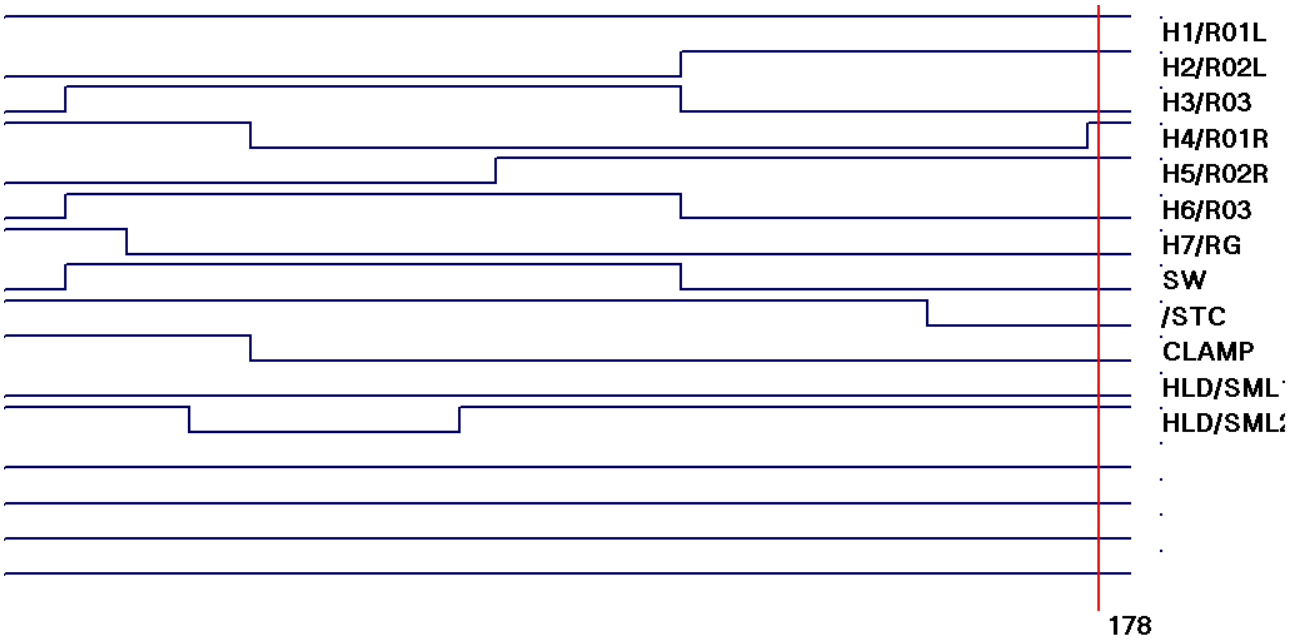


Figure 19 - Phases used for the simulation of the CCD

The clock H2 (or H3) can be used to simulate the CCD signal, the H2 are configured with the low=0v and high=0.5V. The test-cable allows changing the CCD-output-simulated value by using a trimmer.
The out of the cable (**Figure 21** and **Figure 23**) can be connected to the preamplifier board or to the video-bias box, by using the connector in **Figure 20.**

Figure 20 - Adapter to Video-bias box

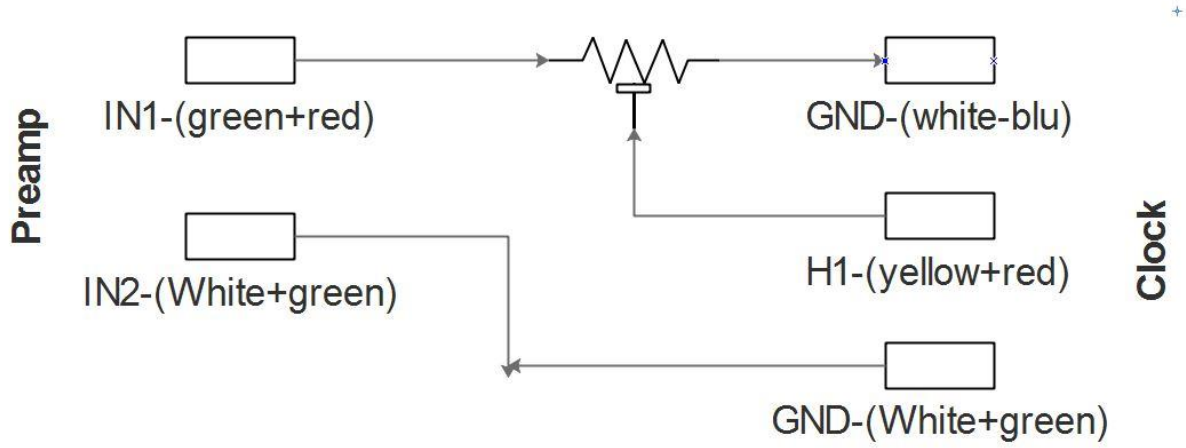


Figure 21 - Schematic of the "CCD simulation" cable

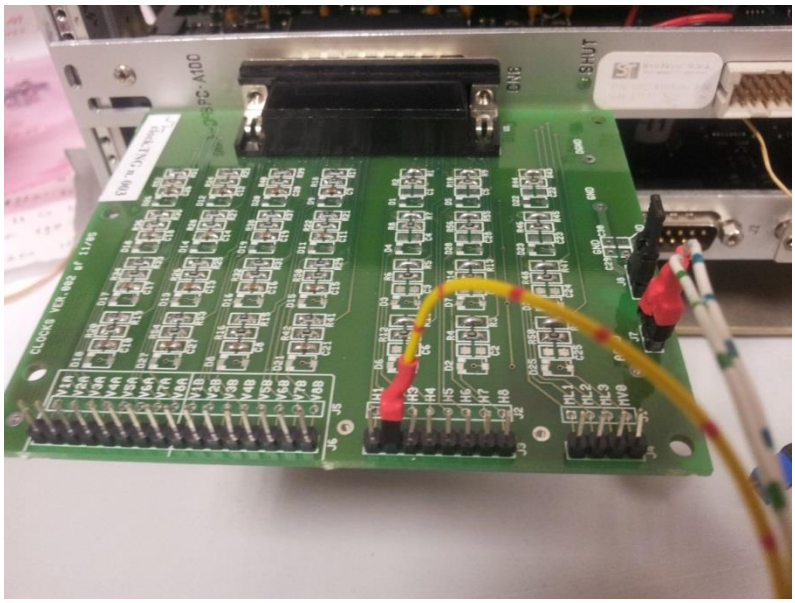


Figure 22 - connection of the CCD simulation cable to the clock board

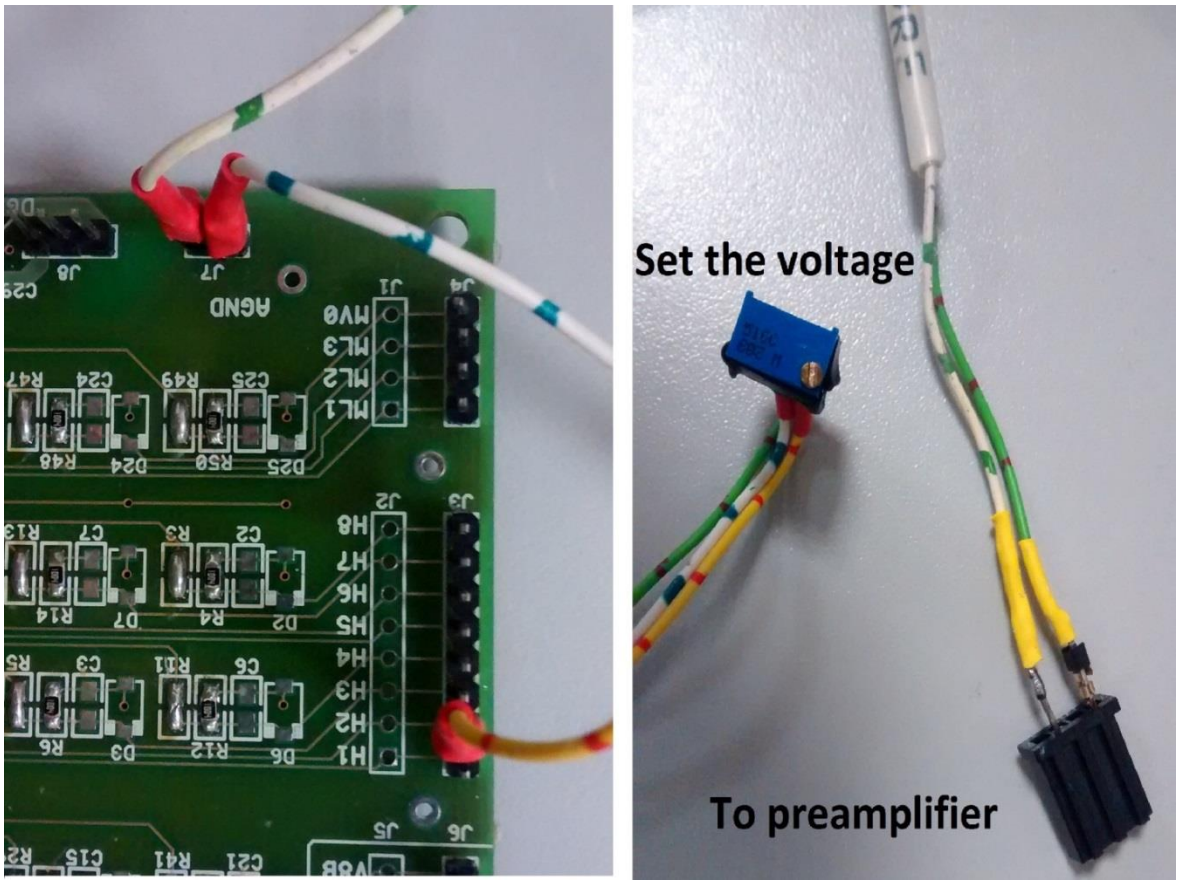


Figure 23 - CCD Simulation cable

The generated signal can be used to set the Input and output offsets of the CCD controller.

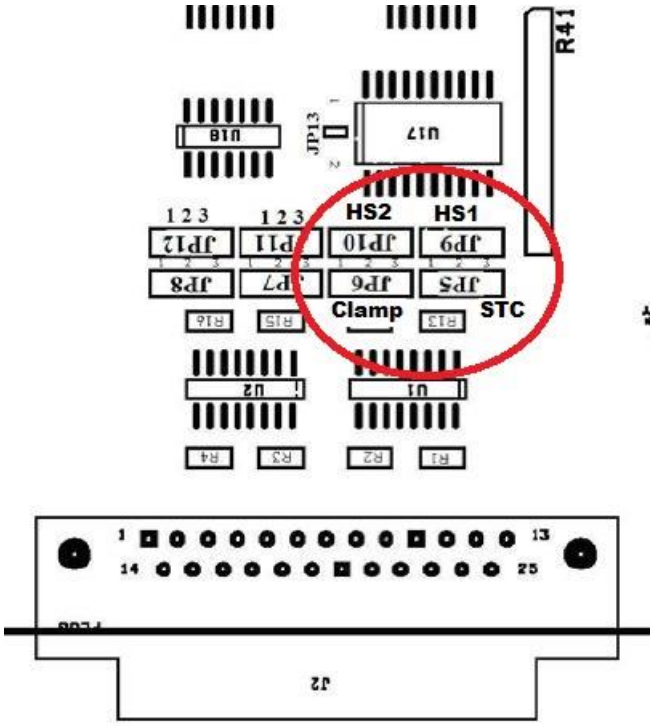


Figure 24 - detail of the CDS board to localize the STC signal

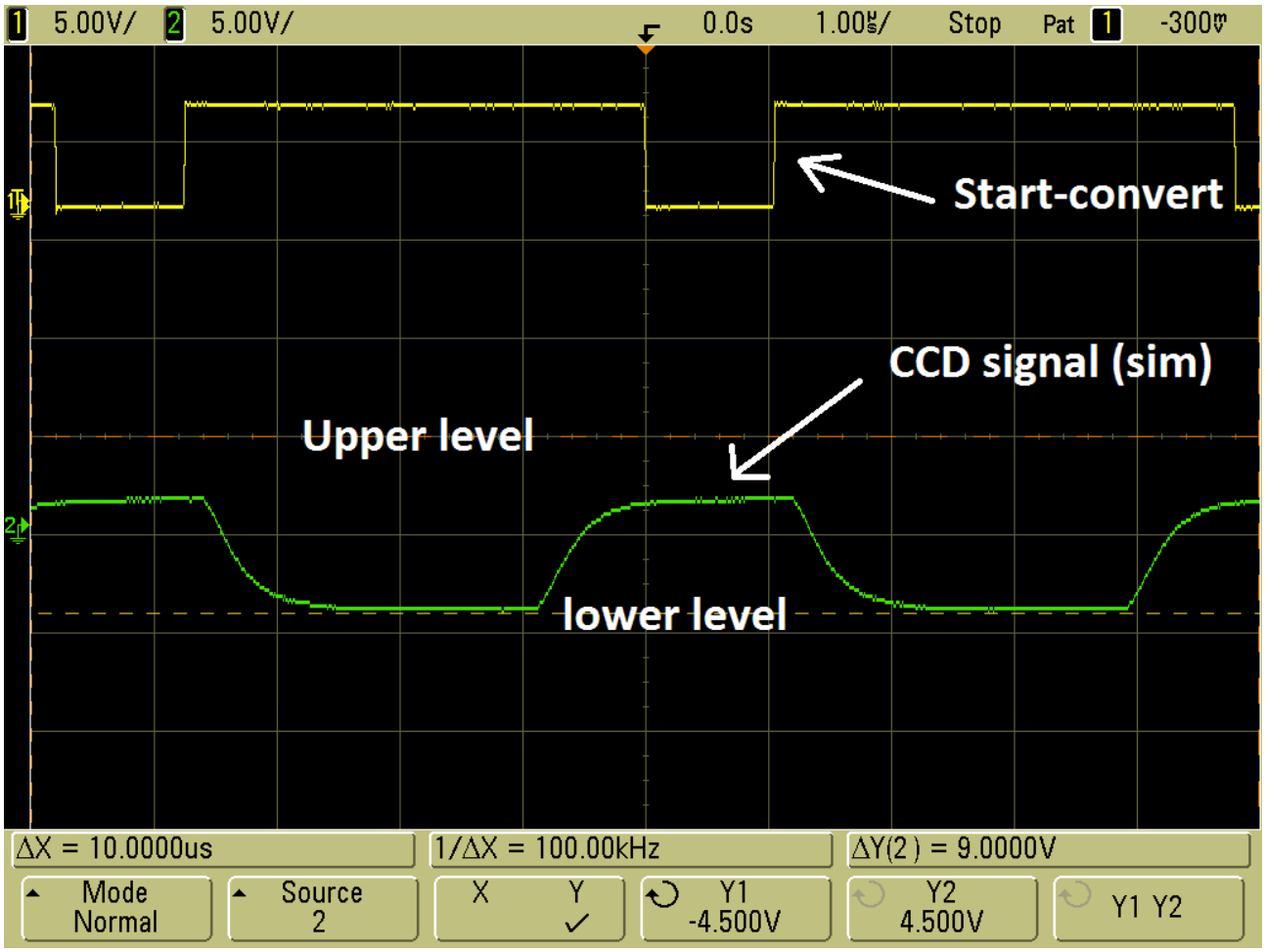
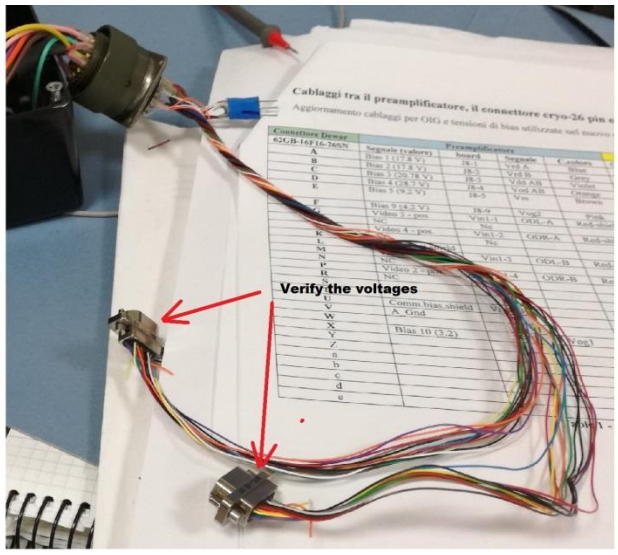


Figure 25 - CCD simulated signal

CCD and front end electronic test

Before the CCD test, an electronic test of the preamplifier and clock boards has to be done.
For this purpose is very important the verification of the voltages and waveform at connector level, before the connection at the CCD.



The voltages have to be compared with the values reported in **Table 5**and **Table 6.**

Table 5 - CCD connection (clock)

Dewar Connector	Clock filter				Nanonics connector (CCD)		Used
62GB-16F16-26SN	Clock	Segnale	C.colors	board	CCD:Pin:conn	Color	
A	H1	R01L	Green/red	J2-1	AB:5:n21	Yellow	YES
B	H2	R02L	Yellow/red	J2-2	AB:4:n21	Orange	YES
C	RET	RET	White/red	AGND			
D	H3	R03-A	Red/black	J2-3	A:6:n21	green	NO
E	H4	R01R	White	J2-4	AB:7:n21	Blue	YES
F	H5	R02R	Black	J2-5	AB:8:n21	Violet	YES
G	H6	R03-B	Red/Blue	J2-6	B:6:n21	green	YES
H							
J	H7	0R-LR	Blue	J2-7	AB:3-9:n21	Red-grey	YES
K	H8	SWRL	Turquoise	J2-8	AB:1-11:n21	Black-black	YES
L	V1	I01-A	Green	J5-9	A:15:n21	yellow	NO
M	V2	I02-A	Pink	J5-10	A:14:n21	Orange	NO
N							
P	V3	I03-A	Orange	J5-11	A:16:n21	green	NO
R	V4	I01-B	Brown	J5-12	B:15:n21	yellow	YES
S	V5	I02-B	Red	J5-13	B:14:n21	Orange	YES
T							
U							
V							
W							
X	V8	DG-B	Grey	J5-16	B:2-10:n21	Brown-white	YES
Y	V7	DG-A	Violet	J5-15	A:2-10:n21	Brown-white	NO
Z							
a	V6	I03-B	Yellow	J5-14	B:16:n21	green	YES
b-c-d-e	NOT USED						

Table 6 - CCD connection (Video-Bias)

Dewar Connector	Preamplifier				Nanonics connector (CCD)		Used
62GB-16F16-26SN	Signal (value)	board	Signal	C.colors	CCD:Pin:conn	Color	
A	Bias 1 (17.8 V)	J8-1	Vrd A	Blue	A:2-7:n15	Brow-blue	NO
B	Bias 2 (17.8 V)	J8-2	Vrd B	Grey	B:2-7:n15	Brow-blue	YES
C	Bias 3 (20.78 V)	J8-3	Vdd AB	Violet	AB:1-8:n15	Black-violet	YES
D	Bias 4 (28.7 V)	J8-4	Vod AB	Orange	AB:9-15:n15	Gray-yellow	YES
E	Bias 5 (9.2 V)	J8-5	Vss	Brown	AB:11-12-13:n15 AB:13-20:n21	Red-brown-black Red-white	YES
F	Bias 9 (4.2 V)	J8-9	Vog2	Pink	AB:3-6:n15	Red-green	YES
G	Video 3 - pos	Vin1-1	ODL-A	Red-shield	A:10:n15	White	NO
H	NC	Nc					
J	Video 4 - pos.	Vin1-2	ODR-A	Red-shield	A:14:n15	Orange	NO
K	NC	Nc					
L	bias.shield						YES
M	Video 1 - pos	Vin1-3	ODL-B	Red-shield	B:10:n15	white	YES
N	NC						
P	Video 2 - pos.	Vin1-4	ODR-B	Red-shield	B:14:n15	Orange	YES
R	NC						
S		Nc					
T		Nc					
U	bias.shield	Vin1234		Black-shield			YES
V	A_Gnd						
W				Turquoise			
X	Bias 10 (3.2)	J8-10	Vog1	Yellow	AB:12-21:n21	Brown-black	YES
Y							
Z							
a							
b							
c							
d							
e							

After the verification of the voltages/waveforms, plug the connectors and test the CCD at room temperature by using the waveforms for the left and right readout.
The acquired images will be saturated images with a well visible CCD overscan.
The next step is a readout test at cryogenic temperature and the setup of the CCD-controller offsets (input and output offset).

Setup of the CCD-Controller offsets (da fare)

Measured gain and conversion factor (da fare)

The CCD gain is calculated using the 'variance method'. I use bias images and couples of images at different exposure time taken in the laboratory. The measures are not very precise because I use a led connected at the shutter driver like light source. The next measure and the tuning of CCD will be done in an optical laboratory.

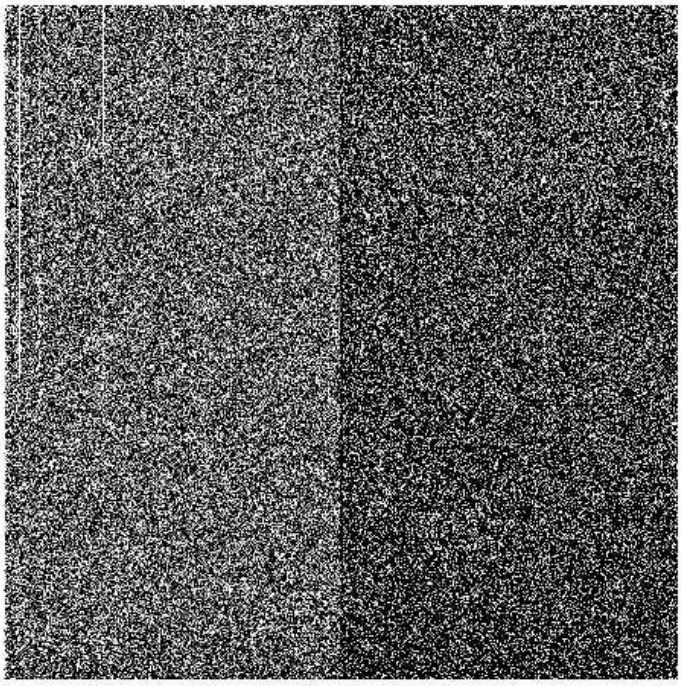


Figure 26 - Bias image (R.M.S. < 8 e^-)

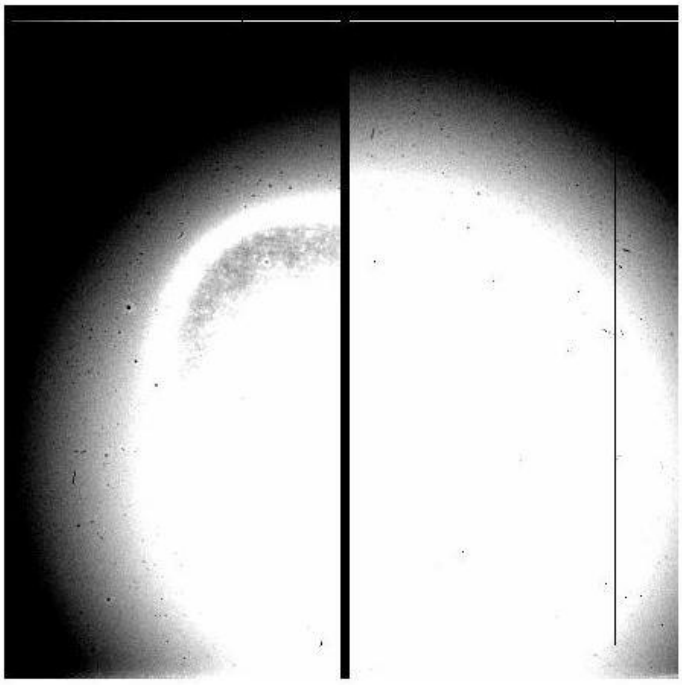


Figure 27 - One of the flat images used for gain calculations

The gain is calculated using 4 pair of images in the dinamic range from 4000 to 35000 ADU.
The measured conversion factor is:

$$FC_{(\text{left ccd})} = 0.91$$
$$FC_{(\text{right ccd})} = 0.83$$

Linearity

The linearities of both ccd are shown in the figures. The deviation from linearity of the left ccd is less than 0.2% in the measured dynamic range, while the deviation of the right ccd is less than 0.17%.
The figures show the value of the measured point as well as the line calculated using the regression method..

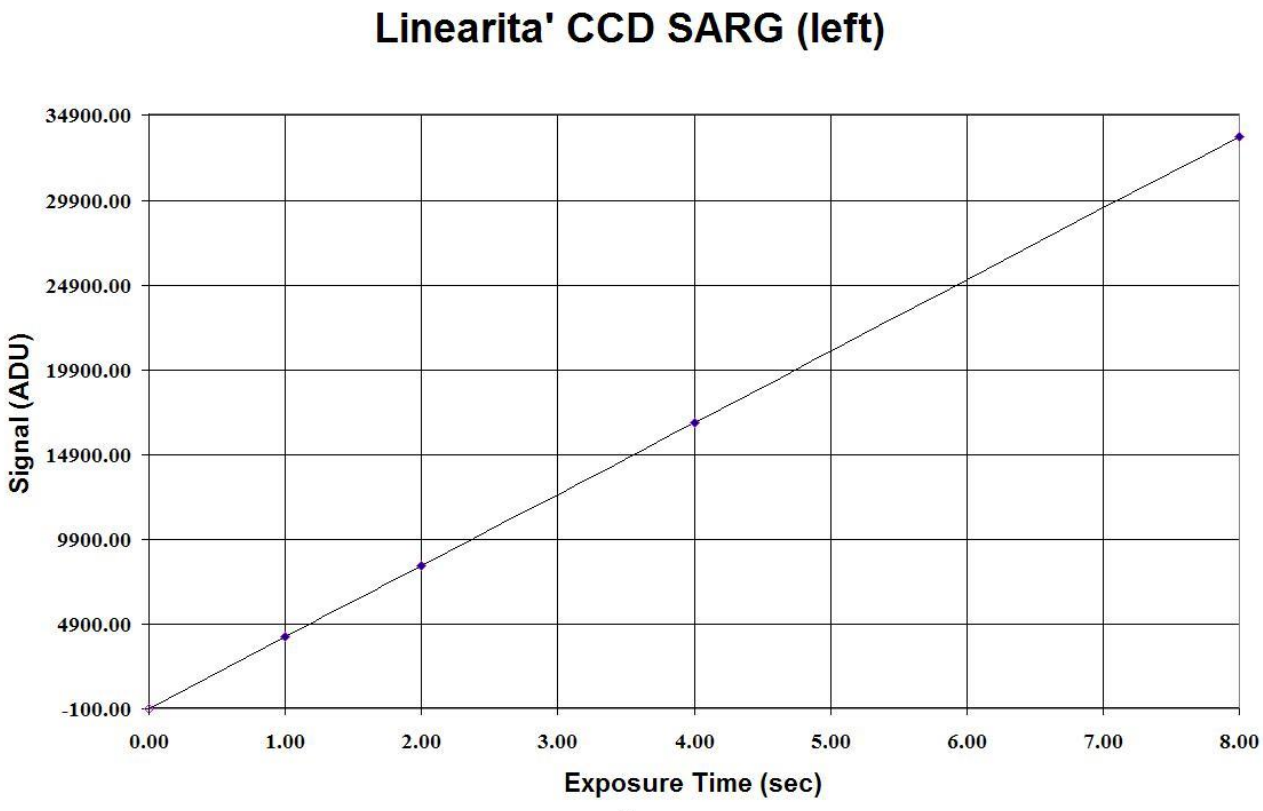


Figura 1 – linearity (left ccd)

Texp (Sec)	Segnale (ADU)	Deviazione Linearità (%)
1	4632.50	0.172
2	9260.50	0.198

4	18601.00	0.073
8	37201.50	0.009

Table 7 - linearity deviation (left ccd)

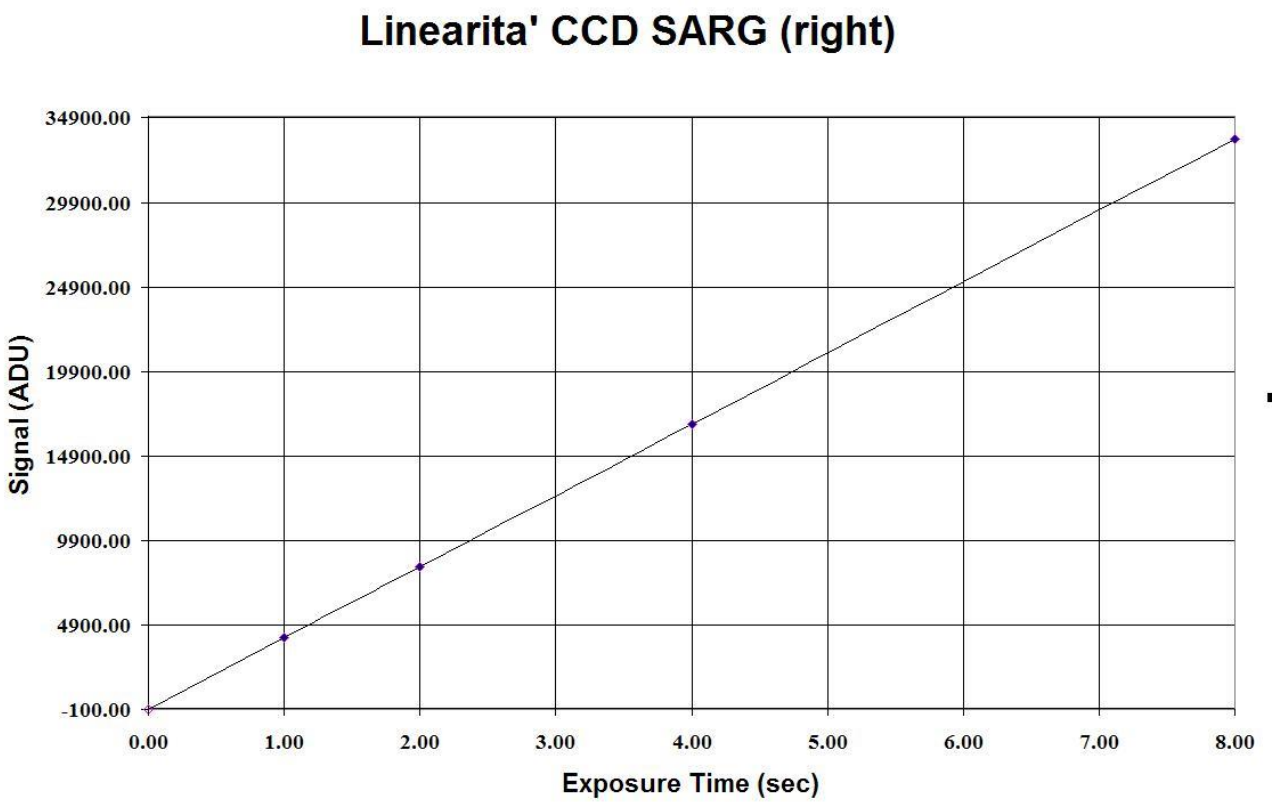


Figure 28 - linearity (right ccd)

Texp (Sec)	Segnale (ADU)	Deviazione Linearità (%)
1	4632.50	0.172
2	9260.50	0.198
4	18601.00	0.073
8	37201.50	0.009

Table 8 – linearity deviation (left ccd)

Measured gain and conversion factor

The CCD gain is calculated using the 'variance method'. I use bias images and couples of images at different exposure time taken in the laboratory. The measures are not very precise because I use a led connected at the shutter driver like light source.
The measures of gain and linearity was done using the '*both*' read mode (four channels simultaneously).

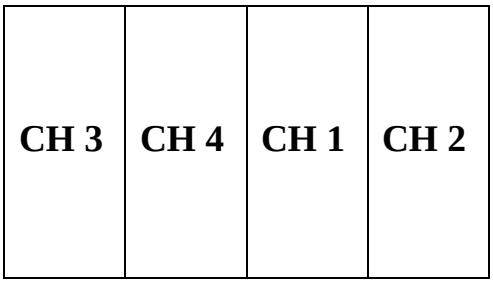


Figure 29 - Read mode 'BOTH' : the result image and the output channels

Gain 2 (default)

$FC_{(ch1)}$ = 0.87 e^- /ADU → r.m.s. = 8.9 e^-
$FC_{(ch2)}$ = 0.85 e^- /ADU → r.m.s. = 7.9 e^-
$FC_{(ch3)}$ = 0.97 e^- /ADU → r.m.s. = 8.7 e^-
$FC_{(ch4)}$ = 1.05 e^- /ADU → r.m.s. = 8.7 e^-

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	3531.00	0.726
2	7079.00	0.037
3	10612.00	0.051
4	14142.50	0.077
5	17676.50	0.113
6	21193.00	0.054
7	24717.00	0.042
8	28234.00	0.009
9	31724.50	0.101

Table 9 - linearity deviation - Channel 1

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	2681.50	0.914
2	5351.00	0.112
3	8017.50	0.119
4	10673.00	0.132
5	13326.00	0.120
6	15974.00	0.082
7	18618.00	0.033
8	21258.00	0.023
9	23890.50	0.098

Table 10 - linearity deviation - Channel 2

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	1830.50	1.310
2	3656.50	0.109
3	5473.50	0.129
4	7288.50	0.220
5	9095.00	0.182
6	10897.50	0.120
7	12691.00	0.005
8	14487.00	0.065
9	16286.50	0.098

Table 11 -linearity deviation - Channel 3

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	2505.50	0.922
2	5004.50	0.105
3	7498.50	0.101
4	9987.00	0.150
5	12467.50	0.115
6	14947.50	0.088
7	17420.50	0.028
8	19891.50	0.026
9	22356.50	0.096

Table 12 - linearity deviation - Channel 4

Gain 1

$FC_{(ch1)}$ = 1.50 e^- /ADU → r.m.s. = 8 e^-
$FC_{(ch2)}$ = 1.46 e^- /ADU → r.m.s. = 11 e^-
$FC_{(ch3)}$ = 1.61 e^- /ADU → r.m.s. = 13.5 e^-
$FC_{(ch4)}$ = 1.73 e^- /ADU → r.m.s. = 12.3 e^-

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	3706.00	3.027
2	7411.00	0.569
3	11127.50	0.353
4	14784.50	0.415
5	18441.50	0.452
6	22071.50	0.355
7	25675.50	0.184
8	29250.00	0.045
9	32756.00	0.434

Table 13 - linearity deviation - Channel 1

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	2576.50	2.202
2	5149.00	0.231
3	7702.00	0.174
4	10248.00	0.310
5	12786.00	0.329
6	15309.50	0.247
7	17814.00	0.083
8	20314.00	0.064
9	22796.50	0.255

Table 14 - linearity deviation - Channel 2

Texp (Sec)	Signal	Linearity

	(ADU)	deviation (%)
1	1364.50	1.940
2	2719.50	0.188
3	4065.00	0.166
4	5406.50	0.271
5	6741.50	0.237
6	8078.50	0.240
7	9404.00	0.119
8	10715.50	0.102
9	12034.50	0.212

Table 15 -linearity deviation - Channel 3

Texp (Sec)	Signal (ADU)	Linearity deviation (%)
1	2330.50	1.651
2	4657.50	0.141
3	6968.00	0.127
4	9276.00	0.235
5	11578.50	0.252
6	13866.50	0.160
7	16146.00	0.041
8	18429.50	0.027
9	20691.00	0.186

Table 16 - linearity deviation - Channel 4

Telescope Test

Measured gain and conversion factor II

The CCD gain is calculated using the 'variance method'. I use bias images and couples of spectra at different exposure time taken at the telescope. I used the following configuration setting:

- Green grism
- Long slit 44000
- No filter
- Green lamp

The measures are not very precise because I use a little rectangular box in the order.
The measures of gain and linearity was done using the '*both*' read mode (four channels simultaneously).

	SARG measured				**Laboratory measured (led)**			
	Binning 1X1		**Binning 2X1**		**Binning 1X1**		**Binning 2X1**	
	CF (e^-/ADU)	r.m.s. (e^-)	CF (e^-/ADU)	r.m.s. (e^-)	CF (e^-/ADU)	r.m.s. (e^-)	CF (e^-/ADU)	r.m.s. (e^-)
CH1	0.82	11	0.81	7.5	0.87	8.9	0.89	6.8
CH2	0.82	10.7	0.83	8.6	0.85	7.9	0.86	10.7
CH3	0.92	10.7	0.93	9.3	0.97	8.7	0.96	12.2

CH4	1	9.5	1.03	10.3	1.05	8.7	1.04	13.3

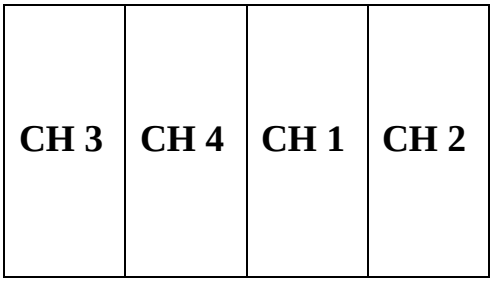


Figure 30 - Read mode 'BOTH' : the result image and the output channels

Test at the telescope

Appendix A (test flow chart)

1) Test led voltages
2) Test the voltages by using the extension board and the **Error! Reference source not f ound.**and **Error! Reference source not found.**
3) Insert the SPC, CDS, cables, bias board and clock board and test the boot, the bias and clock voltages by using the telemetry and tester
   a. Use the following configuration files:
      i. MaxVoltagesBiasClock.ccd
      ii. MeanVoltagesBiasClock.ccd
      iii. MinVoltagesBiasClock.ccd
   b. For each configuration read the telemetry and capture the results
   c. For each configuration read the values with the tester and write the result in …
4) Test the clock values in the High and low state
   a. Use the following configuration files:
      i. testctrl_hi.ccd
      ii. testctrl_low.ccd
   b. For each configuration read the telemetry and capture the results
   c. For each configuration read the values with the tester and write the result in …

5) Test the waveform at the clock board output
   a. Use the “testfasi.ccd” configuration file
   b. Test the horizontal phases with the oscilloscope (time = 500 nSec or 1µsec)
   c. Test the vertical phases with the oscilloscope (time= 20 µsec or 50 µsec)
   d. save the results and put in this report
6) Test the CCD phases
   a. use a real ccd configuration file “”
   b. test the horizontal phase overlap and shape
   c. test the vertical phase overlap and shape
   d. save the results

7) Test the gain an
8) Test the CCD controller with the simulator
9)

Appendix B (Test table)

Rack#	Pre#	CDS#	SPC#

Bias#	Min	Med	Max	OK	Note
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

Clock#	Min	Med	Max	OK	Note
h1					
h2					
h3					
h4					
h5					
h6					
h7					
h8					
V1					
V2					
V3					
V4					
V5					
V6					
V7					
V8					

Channel #	OK	Pre Gain	CDS-G1 Gain	CDS-G2 Gain	CDS-G3 Gain
1					
2					
3					
4					

Appendix C – Document identification code

ORG-TYP-INS-NCOD

ORG = Originator field (i.e. TNG)
TYP = Document Type (see Table 17)
PRJ = project element (see Table 18)
NCOD= numeric code (i.e. 0001)

Example: TNG-MAN-HAN-0001

Table 17 - Document type code

AD	Assumption Document
AN	AN Analysis
COS	Cost Documents (Estimate/CaC/CtC, etc)
DD	Design Description
DP	Data Package
DRD	Document Requirements Description/Definition
DRL	Document Requirements List
DW	Drawing/Diagram
EID	Experiment Interface Document
FI	File (Software/Configuration/Network)
ICD	Interface Control Document
IRD	Interface Requirement Document
ITT	Invitation to Tender
MAN	Manual/User Guide/Handbook
MEM	Memo
MOM	Minutes of Meeting
MOU	Agreement/Memorandum of Understanding
MX	Matrix/Compliance
NCR	Non-Conformance Report
NOT	Note
OPS	Operations Document

PLN	Plan
PO	Proposal
PRE	Progress Report/Status Report
RFQ	Request for Quotation
SOW	Statement of Work
TOR	Terms of Reference
TN	Technical Note
TP	Test Procedure/Test Plan
TR	Test Report/Test Result
TS	Test Specification
VC	Verification Control Document
WBS	Work Breakdown Structure
WP	Working Paper
WPD	Work Package Description

Appendix D – project Element code (to be completed)

Table 18 – Project element code

BTM	Batman
CCD	CCD detector/electronic/software
HAN	HARPSN
TRK	Tracking

Appendix E – List of acronyms (Example)

CCD	Charge Coupled Device
CDS	Correlated Double Sampling
TBC	To Be Confirmed
TBD	To Be defined
TBF	To be fixed
TNG	Telescopio Nazionale Galileo